PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER USING AUTOMATIC LOOP CONTROL AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

A phase-locked loop (PLL) frequency synthesizer comprising: 1) a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by the frequency control voltage level; 2) a first frequency divider for dividing the operating frequency, Fout, of the output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N; 3) a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M; and 4) a phase-frequency detector for comparing the first and second divided clock signals and generating an UP control signal if the first divided clock signal is slower than the second divided clock signal and generating a DOWN control signal if the first divided clock signal is faster than the second divided clock signal. The PLL frequency synthesizer further comprises: 5) a charge pump for receiving the UP and DOWN control signals and increasing the frequency control voltage level on the loop filter by injecting a charge pump current, Ic, and decreasing the frequency control voltage level on the loop filter by draining the charge pump current, Ic; and 6) a loop

response control circuit for adjusting a value of Ic as a function of the first divider value, N, and the second divider value, M.